Besides, the present invention is applicable not only to the semiconductor laser but also to the manufacture of a light emitting diode. Furthermore, this invention is applicable to the manufacture of various semiconductor devices having layers of p-type nitride-based Group III-V compounds. Other modifications may be made to the invention without departing from the spirit of the invention.

As has been described above, according to the present invention, the acceptor-doped AlN or Al_2O_3 cap layer is formed on the acceptor-doped nitride-based Group III-V compound semiconductor layer, and the resultant structure is subjected to heat treatment. Thus, the heat treatment temperature is raised and hydrogen can be removed while curbing evaporation of a constituent element such as nitrogen. Therefore, the electrical activation ratio of acceptor impurity in the nitride-based Group III-V compound semiconductor layer can be increased and the high-quality p-type layer can be formed. This contributes to realization of a high-performance, short-wavelength semiconductor laser, etc.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A semiconductor device comprising:

a buffer semiconductor layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leqq s \leqq 1$, $0 \leqq t \leqq 1$, $s+t \leqq 1$) and having a number of pinholes formed therein;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $u+v \leqq 1$) formed on said buffer semiconductor layer and having a different chemical formula from that of said buffer semiconductor layer,

a first cladding layer formed on said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

2. The semiconductor device according to claim 1, wherein, in said $Al_{1-u-v}Ga_uIn_vN$ ($0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $u+v \leqq 1$) for said thermal distortion reducing layer, v is set to be not less than 0.1 and not more than 0.9.

3. A semiconductor device according to claim 1, wherein a film thickness of said thermal distortion reducing layer is greater than that of said semiconductor layer.

4. The semiconductor device according to claim 1, further comprising a cap layer on said thermal distortion reducing layer to prevent evaporation of In included in said thermal distortion reducing layer.

5. The semiconductor device according to claim 4, wherein said cap layer is made of $Al_{1-x}Ga_xN$ ($0 \leqq x \leqq 1$) and is formed at 500° C. to 800° C.

6. The semiconductor device according to claim 1, wherein said first cladding layer is made of $Al_{1-x-y}Ga_xIn_yN$ ($0 \leqq x \leqq 1$, $0 \leqq y \leqq 1$, $x+y \leqq 1$).

7. The semiconductor device according to claim 1, wherein said thermal distortion reducing layer has a thickness of 50 nm to 1000 nm.

8. A semiconductor device according to claim 1, further comprising a single crystal substrate on which said semiconductor layer is formed.

9. A semiconductor laser comprising:

a first layer;

a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leqq u \leqq 1$, $0 \leqq v \leqq 1$, $u+v \leqq 1$) formed on said first layer,

a third layer formed on said second layer;

an active layer formed on said third layer; and

a fourth layer formed on said active layer,

wherein said first layer is formed of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leqq s \leqq 1$, $0 \leqq t \leqq 1$, $s+t \leqq 1$)with an average film thickness of 3 nm to 10 nm such that said first layer has a number of pinholes formed among said $Al_{1-s-t}Ga_sIn_tN$ ($0 \leqq s \leqq 1$, $0 \leqq t \leqq 1$, $s+t \leqq 1$).

10. A secmiconductor laser according to claim 9, further comprising a single crystal substrate on which said first layer is formed.

* * * * *

11. The semiconductor device according to claim 1, comprising:

a substrate;

said buffer semiconductor layer being formed on said substrate; and

said pinholes comprising exposed portions of said substrate through said buffer semiconductor layer.

12. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer comprises crystals formed spaced apart; and

said pinholes comprise spaces between said crystals.

13. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer comprises crystals loosely formed; and

said pinholes comprise spaces between said crystals.

14. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer consists essentially of an AlGaN material.

15. The semiconductor device according to claim 1, wherein:

said buffer semiconductor layer consists essentially of an AlN material.

16. The semiconductor device according to claim 1, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

17. A semiconductor device comprising:

a substrate;

crystals formed on said substrate containing at least Al and N;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u < 1$, $0 \leq v < 1$, $u+v<1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

18. The semiconductor device according to claim 17, wherein:

said crystals being disposed to expose portions of said substrate.

19. The semiconductor device according to claim 17, wherein:

said crystals being loosely formed on said substrate.

20. The semiconductor device according to claim 17, wherein:

said crystals comprise means for controlling polarity.

21. The semiconductor device according to claim 17, wherein:

said crystals consists essentially of an AlGaN material.

22. The semiconductor device according to claim 17, wherein:

said crystals consists essentially of an AlN material.

23. The semiconductor device according to claim 17, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

24. A semiconductor device comprising:

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$) and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of a growth surface.

25. A semiconductor device according to claim 24, wherein:

said means comprises pinholes.

26. A semiconductor device according to claim 24, wherein:

said means comprises a shape of said buffer layer.

27. The semiconductor device according to claim 24, further comprising:

a substrate, wherein:

said buffer layer comprises crystals formed on said substrate; and

said means comprises intervals between said crystals exposing said substrate.

28. The semiconductor device according to claim 24, wherein:

said buffer layer consists essentially of an AlGaN material.

29. The semiconductor device according to claim 24, wherein:

said buffer layer consists essentially of an AlN material.

30. The semiconductor device of claim 24, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

31. A semiconductor device comprising:

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$)

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of growth surface of said thermal distortion reducing layer.

32. A semiconductor device according to claim 31, wherein:

said means comprises pinholes.

33. A semiconductor device according to claim 31, wherein:

said means comprises a shape of said buffer layer.

34. The semiconductor device according to claim 31, further comprising:

a substrate, wherein:

said buffer layer comprises crystals formed on said substrate; and

said means comprises intervals between said crystals exposing said substrate.

35. The semiconductor device according to claim 31, wherein:

said buffer layer consists essentially of an AlGaN material.

36. The semiconductor device according to claim 31, wherein:

said buffer layer consists essentially of an AlN material.

37. The semiconductor device of claim 31, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

38. A semiconductor device manufactured using a process comprising:

growing a first buffer layer of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$) on a surface of a substrate having portions exposing said surface of said substrate;

forming a second buffer layer of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) on said first buffer layer and having a different chemical formula from that of said first buffer layer; and

forming an active layer over said second buffer layer.

39. A device according to claim 38, wherein said process comprises:

growing said first buffer layer at a temperature between and 350 C and 800 C.

40. A device according to claim 38, wherein said process comprises:

forming said second buffer layer to absorb thermal distortion.

41. A device according to claim 38, wherein said process comprises:

forming said first buffer layer consisting essentially of AlGaN.

42. A device according to claim 38, wherein said process comprises: forming said first buffer layer consisting essentially of AlN.

43. A device according to claim 38, wherein said process comprises: forming said second buffer layer consisting essentially of GaN.

44. A device according to claim 38, wherein said process comprises: forming said first buffer layer as spaced crystals.